

# DATA SHEET

## **BLF543** UHF power MOS transistor

Product specification

October 1992

# UHF power MOS transistor

# BLF543

## FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

## DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the UHF frequency range.

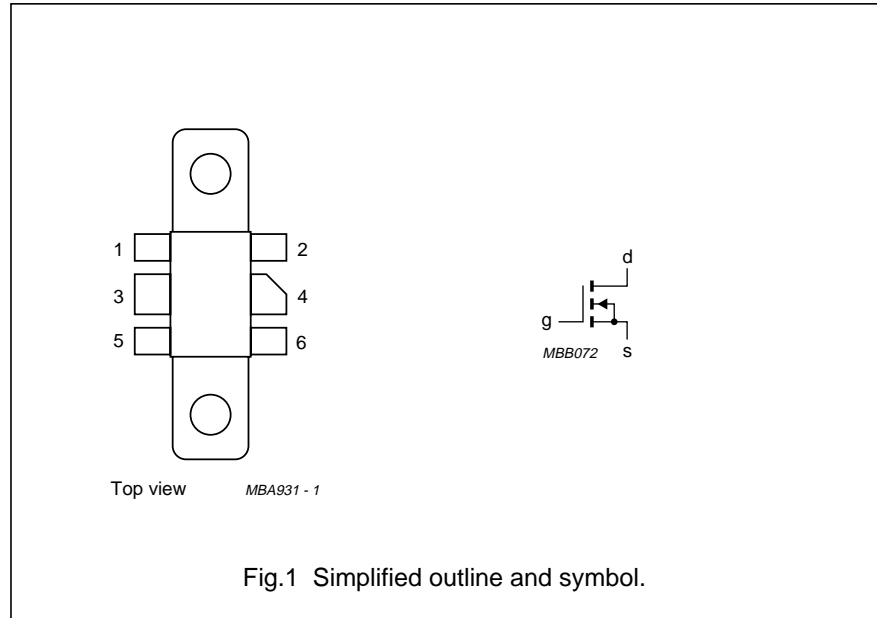
The transistor is encapsulated in a 6-lead, SOT171 flange envelope, with a ceramic cap. All leads are isolated from the flange.

The devices are marked with a  $V_{GS}$  indication intended for matched pair applications.

## PINNING - SOT171

PIN	DESCRIPTION
1	source
2	source
3	gate
4	drain
5	source
6	source

## PIN CONFIGURATION



## CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

## WARNING

**Product and environmental safety - toxic materials**

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

## QUICK REFERENCE DATA

RF performance at  $T_h = 25\text{ }^\circ\text{C}$  in a common source class-B circuit.

MODE OF OPERATION	f (MHz)	$V_{DS}$ (V)	$P_L$ (W)	$G_p$ (dB)	$\eta_D$ (%)
CW, class-B	500	28	10	> 12	> 50
CW, class-B	960	28	10	typ. 8	typ. 50

# UHF power MOS transistor

BLF543

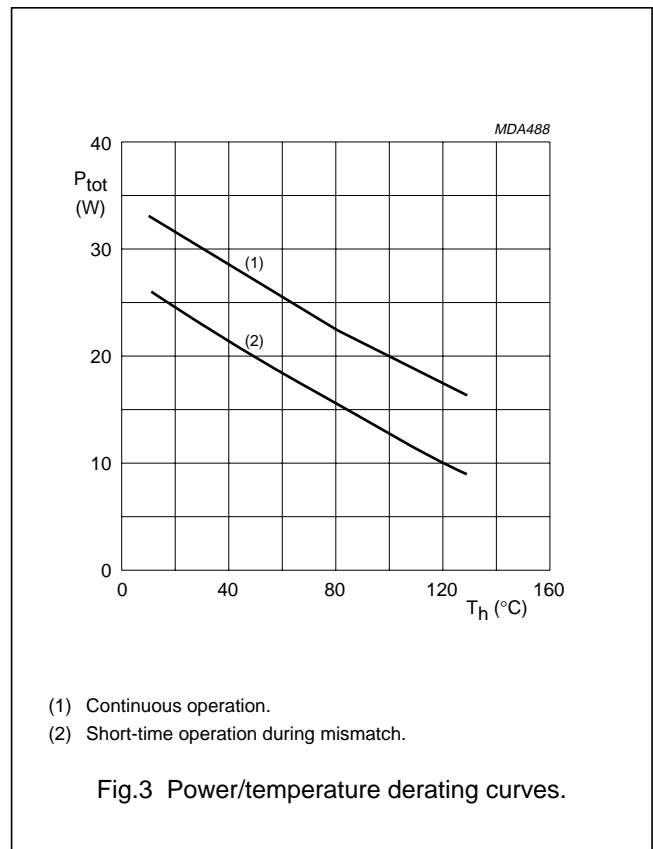
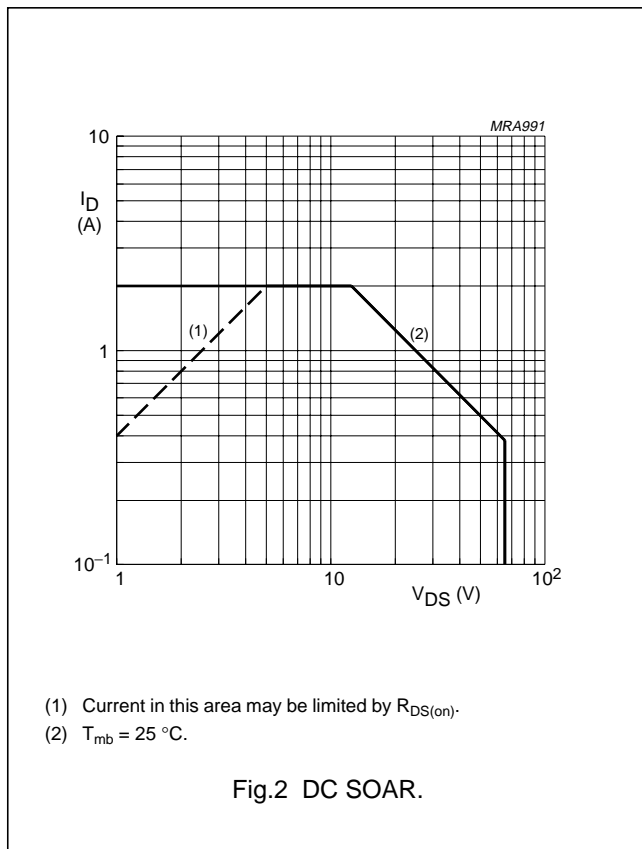
## LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
$I_D$	DC drain current		–	2	A
$P_{tot}$	total power dissipation	up to $T_{mb} = 25\text{ }^\circ\text{C}$	–	25	W
$T_{stg}$	storage temperature		–65	150	$^\circ\text{C}$
$T_j$	junction temperature		–	200	$^\circ\text{C}$

## THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-mb}$	thermal resistance from junction to mounting base	7 K/W
$R_{th\ mb-h}$	thermal resistance from mounting base to heatsink	0.4 K/W



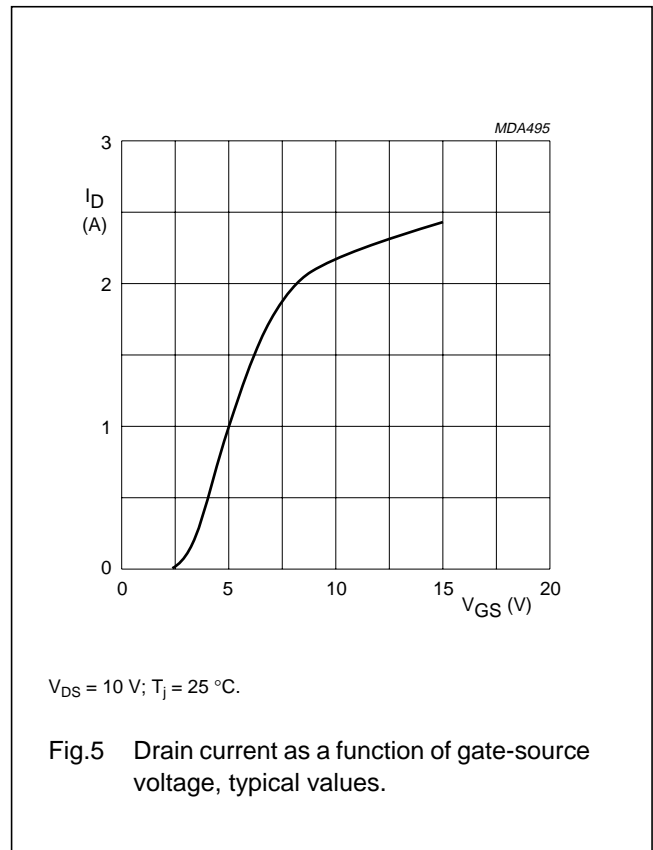
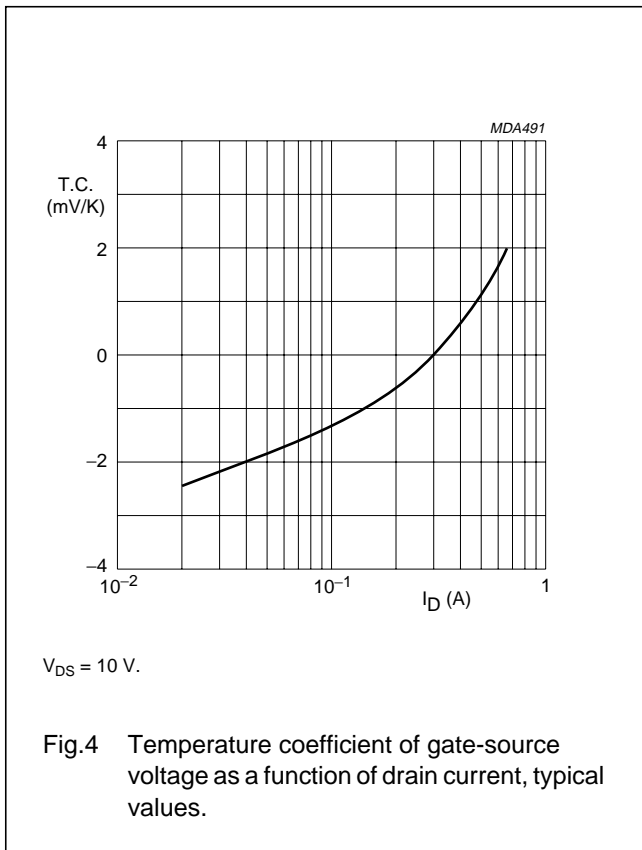
UHF power MOS transistor

BLF543

**CHARACTERISTICS**

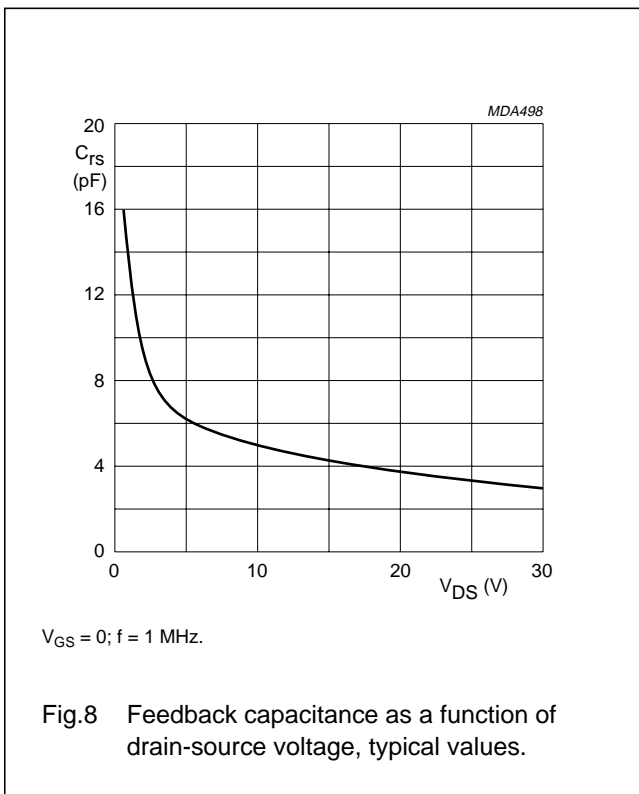
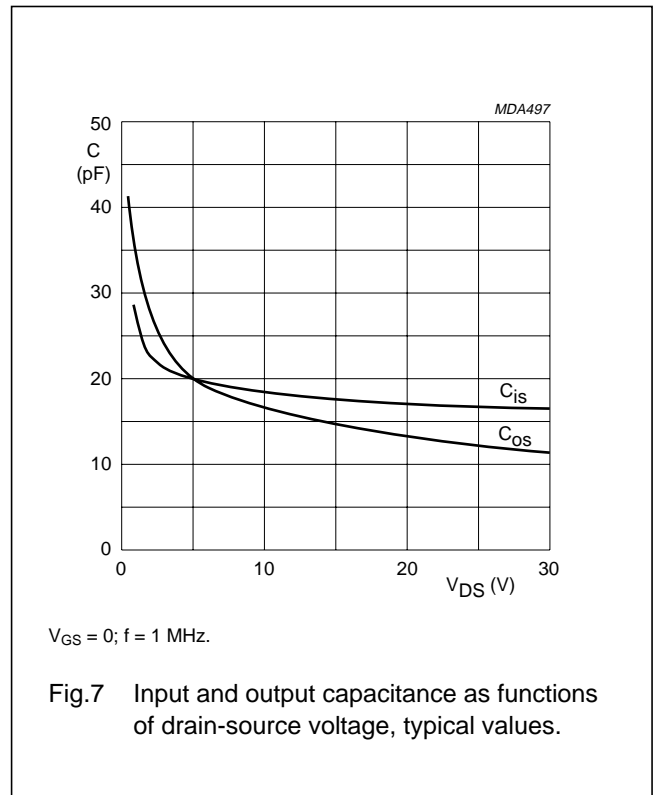
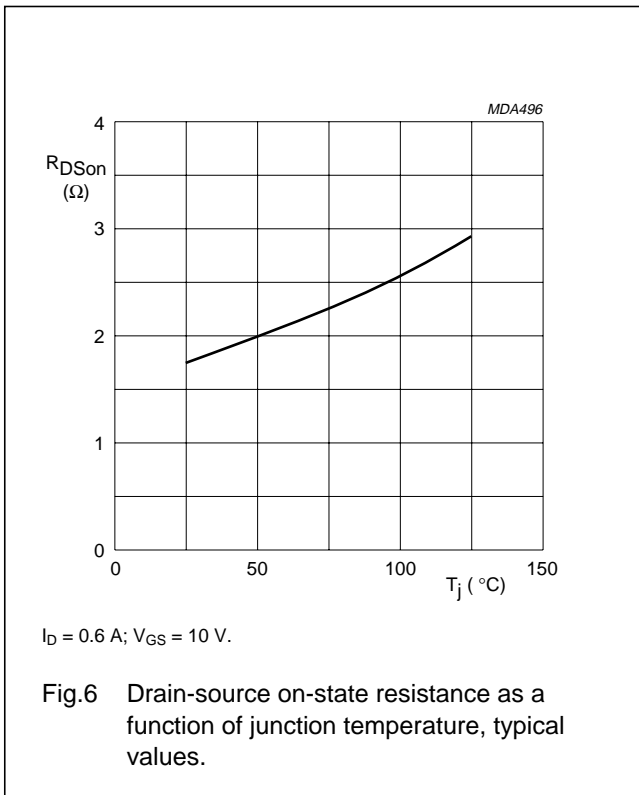
$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0; I_D = 5\text{ mA}$	65	–	–	V
$I_{DSS}$	drain-source leakage current	$V_{GS} = 0; V_{DS} = 28\text{ V}$	–	–	0.5	mA
$I_{GSS}$	gate-source leakage current	$\pm V_{GS} = 20\text{ V}; V_{DS} = 0$	–	–	1	$\mu\text{A}$
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 20\text{ mA}; V_{DS} = 10\text{ V}$	1	–	4	V
$\Delta V_{GS(th)}$	gate-source voltage difference of matched pairs	$I_D = 20\text{ mA}; V_{DS} = 10\text{ V}$	–	–	100	mV
$g_{fs}$	forward transconductance	$I_D = 0.6\text{ A}; V_{DS} = 10\text{ V}$	300	450	–	mS
$R_{DS(on)}$	drain-source on-state resistance	$I_D = 0.6\text{ A}; V_{GS} = 10\text{ V}$	–	1.7	2.5	$\Omega$
$I_{DSX}$	on-state drain current	$V_{GS} = 15\text{ V}; V_{DS} = 10\text{ V}$	–	2.4	–	A
$C_{is}$	input capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	16	–	pF
$C_{os}$	output capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	12	–	pF
$C_{rs}$	feedback capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	3.2	–	pF



UHF power MOS transistor

BLF543



# UHF power MOS transistor

# BLF543

## APPLICATION INFORMATION FOR CLASS-B OPERATION

$T_h = 25\text{ }^\circ\text{C}$ ;  $R_{th\text{ mb-h}} = 0.4\text{ K/W}$ , unless otherwise specified.

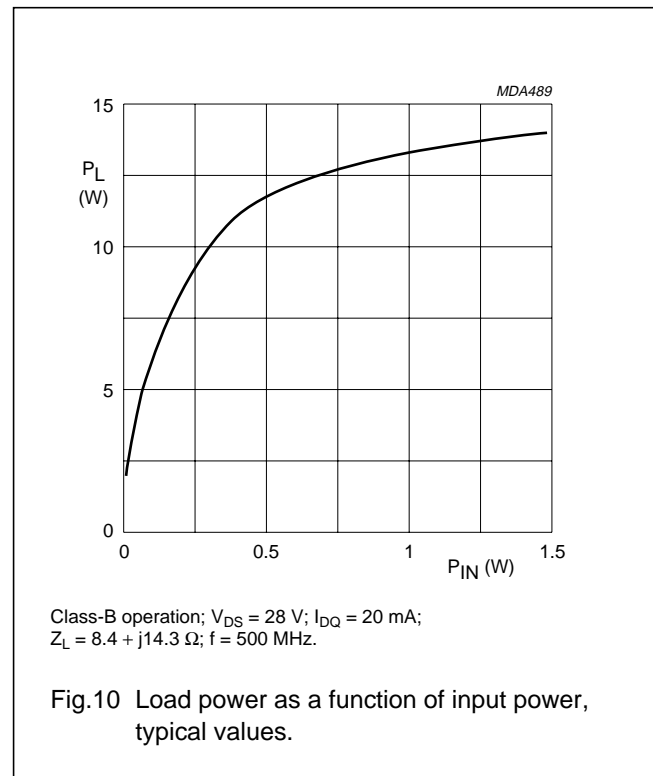
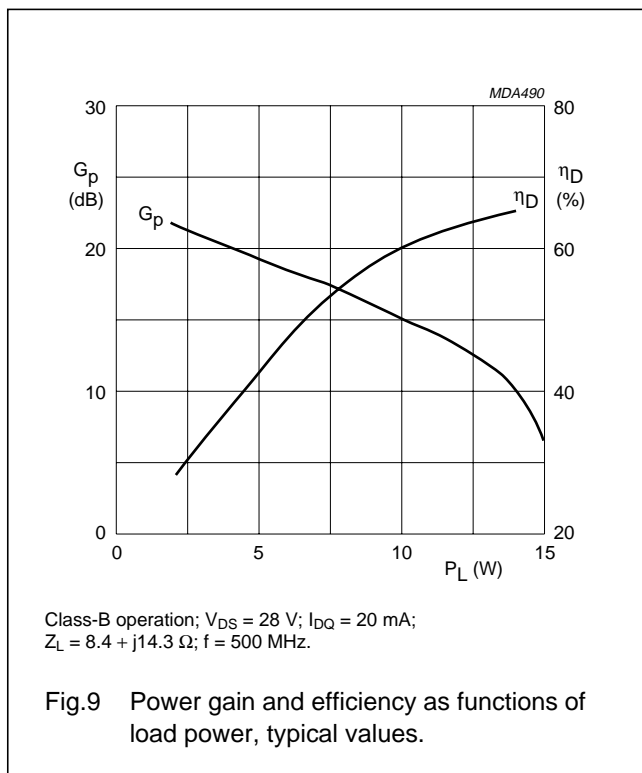
RF performance in a common source class-B circuit.

MODE OF OPERATION	f (MHz)	V <sub>DS</sub> (V)	I <sub>DQ</sub> (mA)	P <sub>L</sub> (W)	G <sub>p</sub> (dB)	η <sub>D</sub> (%)
CW class-B	500	28	20	10	> 12 typ. 15	> 50 typ. 60
CW class-B	960	28	20	10	typ. 8	typ. 50
CW class-B	960	24	20	7.5	typ. 8	typ. 50

### Ruggedness in class-B operation

The BLF543 is capable of withstanding a full load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V<sub>DS</sub> = 28 V; f = 500 MHz at rated output power.



UHF power MOS transistor

BLF543

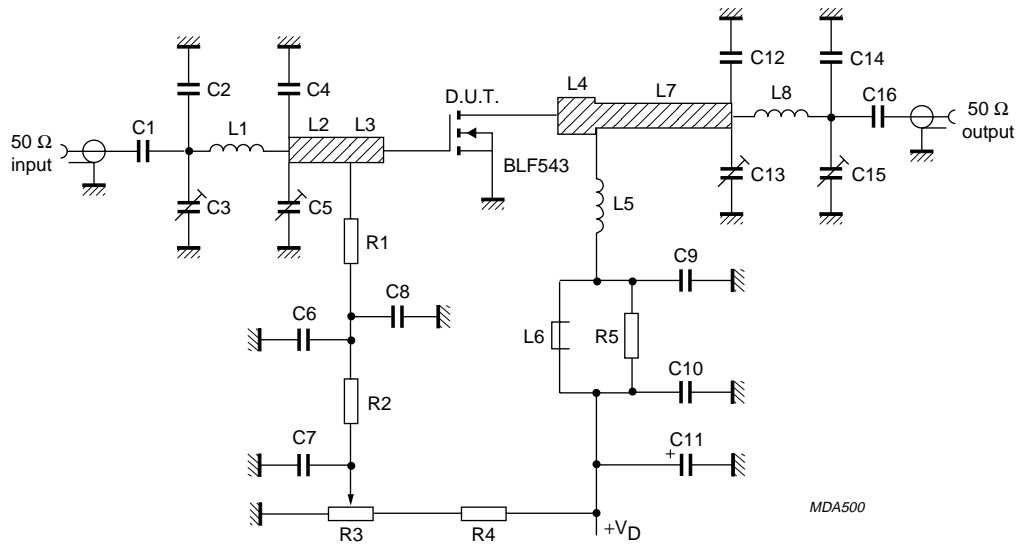


Fig.11 Test circuit for class-B operation at 500 MHz.

## UHF power MOS transistor

BLF543

## List of components (class-B test circuit at 500 MHz)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C6, C9, C16	multilayer ceramic chip capacitor (note 1)	390 pF		
C2, C14	multilayer ceramic chip capacitor (note 1)	7.5 pF		
C3, C5, C13, C15	film dielectric trimmer	9 pF		2222 809 09002
C4	multilayer ceramic chip capacitor (note 1)	20 pF		
C7	multilayer ceramic chip capacitor	2 × 100 nF in parallel, 50 V		2222 852 47104
C8, C10	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C11	aluminium electrolytic capacitor	10 µF, 63 V		2222 030 28109
C12	multilayer ceramic chip capacitor (note 1)	22 pF		
L1	1 turn enamelled 0.8 mm copper wire	11 nH	int. dia. 4.7 mm leads 2 × 5 mm	
L2	stripline (note 2)	42.5 Ω	14.5 × 3 mm	
L3, L4	stripline (note 2)	42.5 Ω	6 × 3 mm	
L5	7 turns enamelled 1 mm copper wire	124 nH	length 7.8 mm int. dia. 4 mm leads 2 × 5 mm	
L6	grade 3B Ferroxcube RF choke			4312 020 36640
L7	stripline (note 2)	55.7 Ω	31 × 2 mm	
L8	1 turn enamelled 1 mm copper wire	8 nH	int. dia. 3.2 mm leads 2 × 5 mm	
R1, R2	0.4 W metal film resistor	1 kΩ		2322 151 71002
R3	10 turns cermet potentiometer	5 kΩ		
R4	0.4 W metal film resistor	19.6 kΩ		2322 151 71963
R5	1 W metal film resistor	10 Ω		2322 153 51009

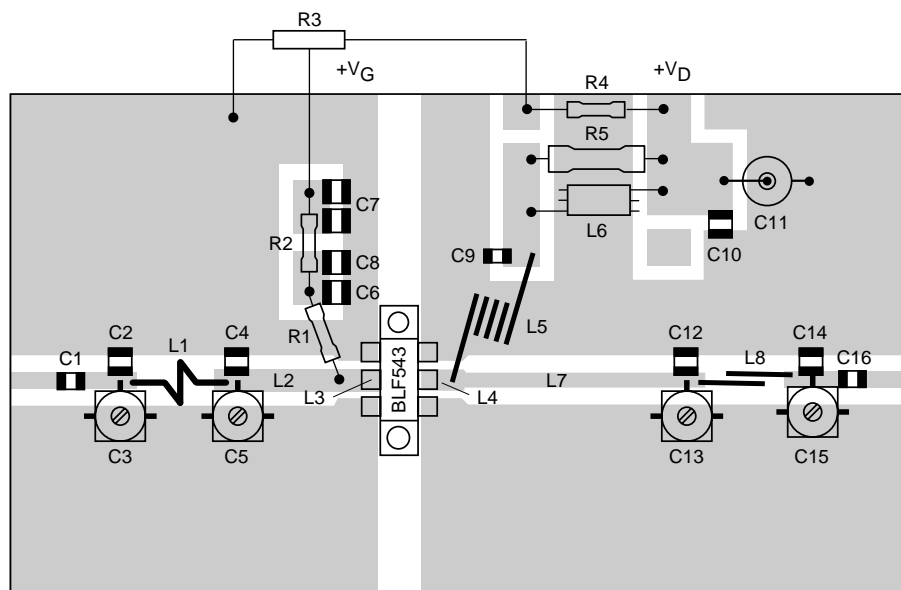
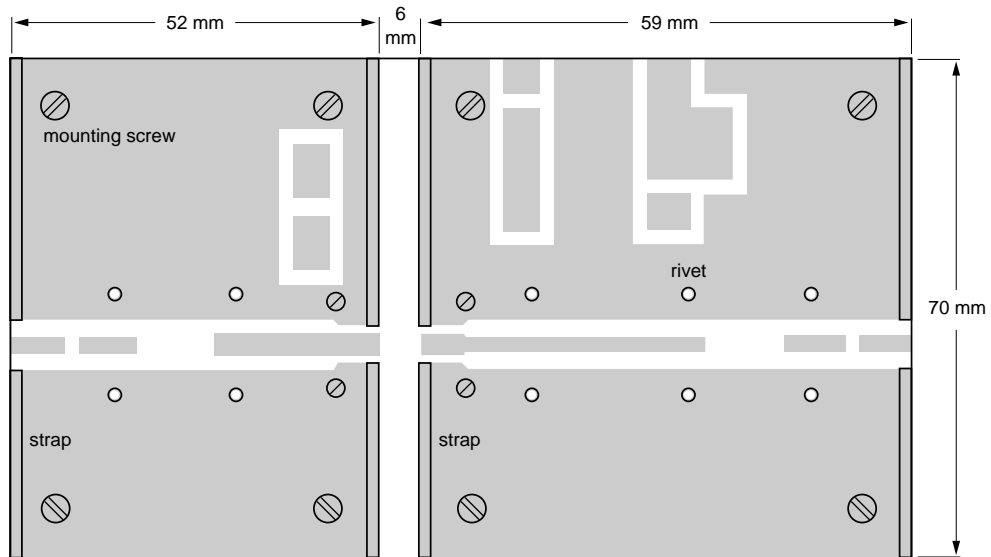
## Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with glass microfibre reinforced PTFE ( $\epsilon_r = 2.2$ ); thickness  $\frac{1}{32}$  inch.



UHF power MOS transistor

BLF543



MDA487

The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz class-B test circuit.

UHF power MOS transistor

BLF543

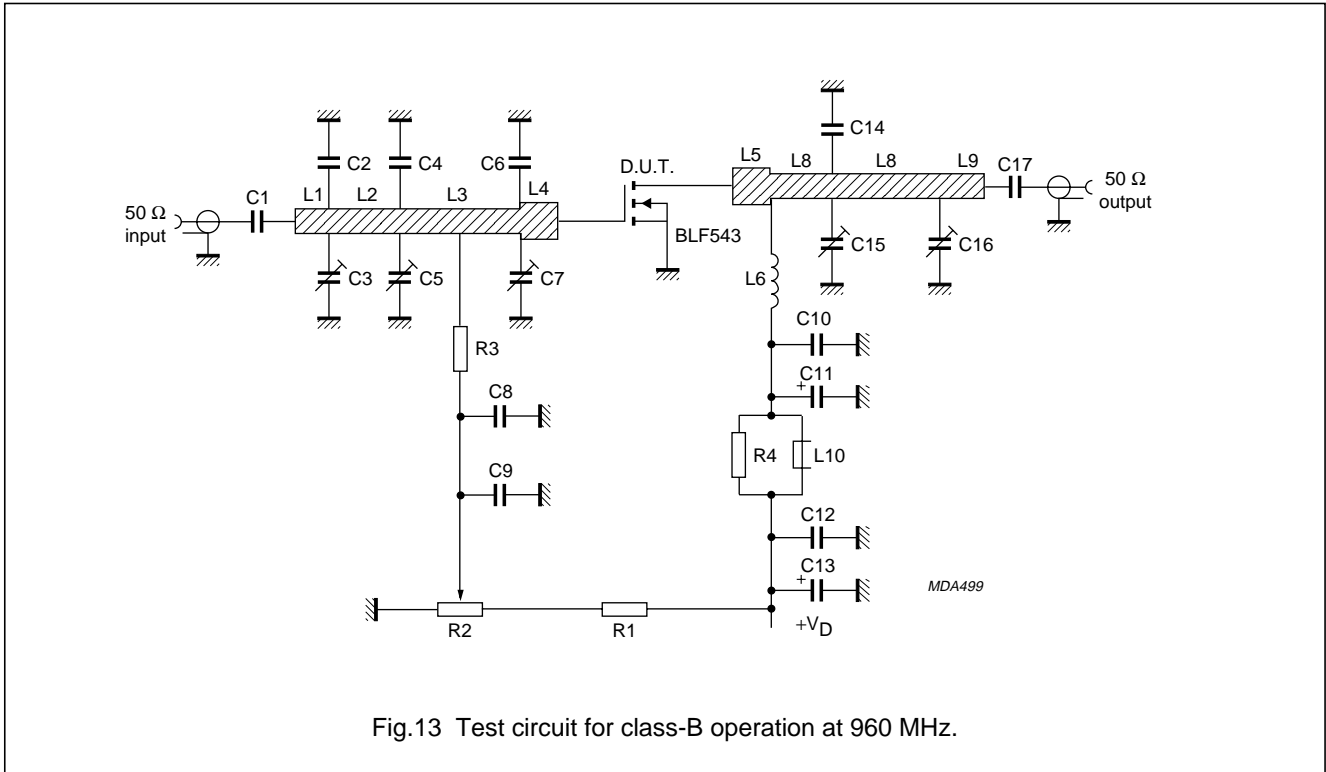


Fig.13 Test circuit for class-B operation at 960 MHz.

## UHF power MOS transistor

BLF543

## List of components (class-B test circuit at 960 MHz)

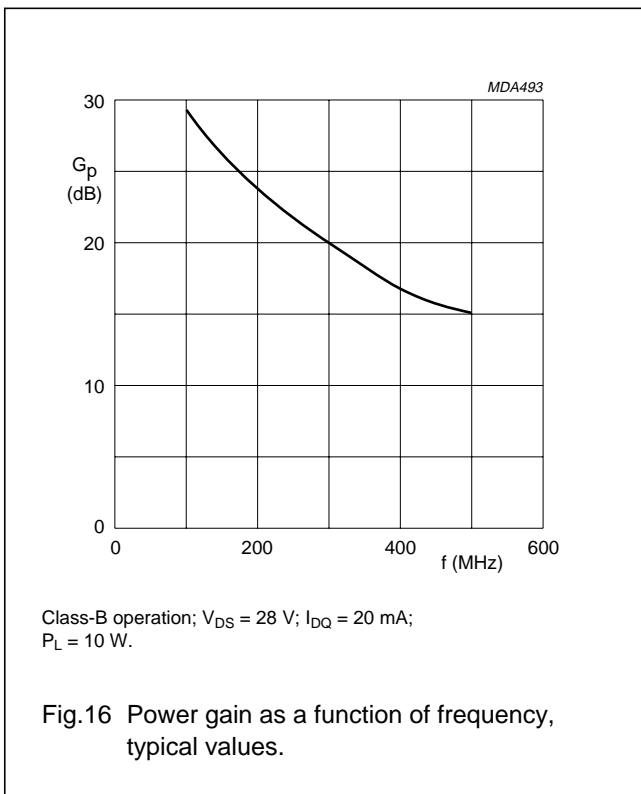
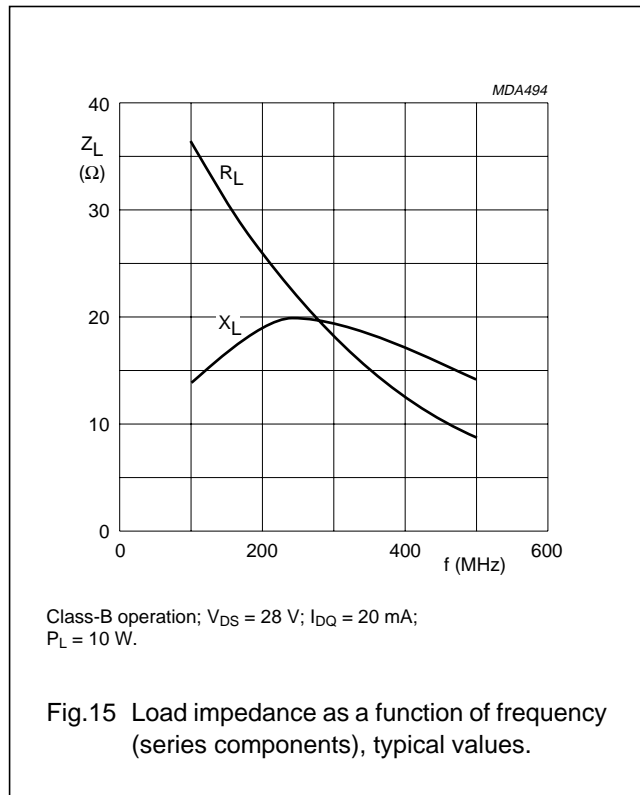
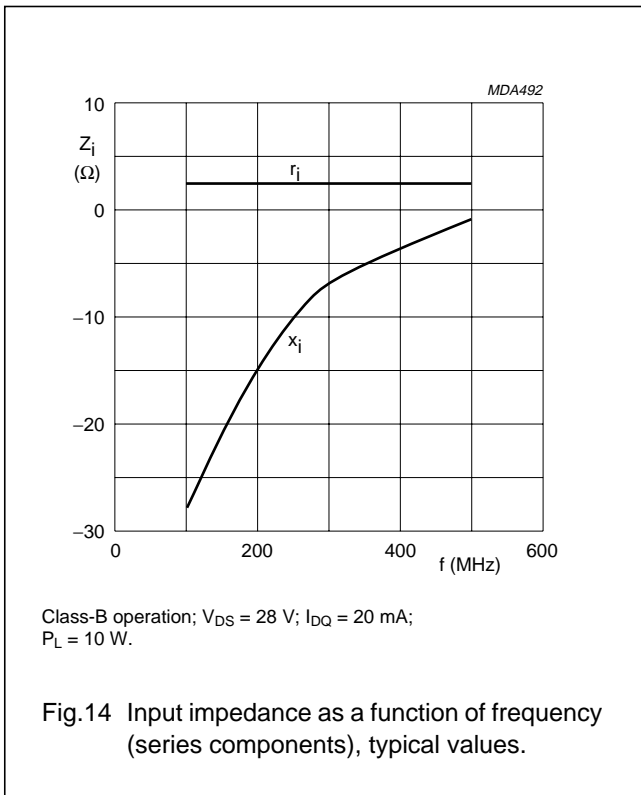
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C8, C10, C17	multilayer ceramic chip capacitor (note 1)	68 pF		
C2	multilayer ceramic chip capacitor (note 2)	4.7 pF		
C3, C5, C15, C16	film dielectric trimmer	1.2 to 5.5 pF		2222 808 00004
C4	multilayer ceramic chip capacitor (note 2)	2 × 5.6 pF in parallel		
C6, C7	multilayer ceramic chip capacitor (note 2)	7.5 pF		
C9, C12	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C14	multilayer ceramic chip capacitor (note 2)	2 × 4.7 pF in parallel		
C11, C13	aluminum electrolytic capacitor	10 μF, 63 V		2222 030 28109
L1	stripline (note 3)	50 Ω	12.5 × 2.5 mm	
L2	stripline (note 3)	50 Ω	19 × 2.5 mm	
L3	stripline (note 3)	50 Ω	29.5 × 2.5 mm	
L4, L5	stripline (note 3)	42.5 Ω	3 × 3 mm	
L6	3 turns enamelled 0.8 mm copper wire	35 nH	length 4.6 mm int. dia. 4 mm leads 2 × 5 mm	
L7	stripline (note 3)	50 Ω	12.5 × 2.5 mm	
L8	stripline (note 3)	50 Ω	28.5 × 2.5 mm	
L9	stripline (note 3)	50 Ω	20.5 × 2.5 mm	
L10	grade 3B Ferroxcube RF choke			4312 020 36640
R1	0.4 W metal film resistor	205 kΩ		2322 151 72054
R2	10 turns potentiometer	50 kΩ		
R3	0.4 W metal film resistor	10 kΩ		2322 151 71003
R4	0.4 W metal film resistor	10 Ω		2322 153 51009

## Notes

- American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
- American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
- The striplines are on a double copper-clad printed circuit board, with glass microfibre reinforced PTFE ( $\epsilon_r = 2.2$ ); thickness  $\frac{1}{32}$  inch.

UHF power MOS transistor

BLF543



**Optimum input and load impedances**

Optimum input impedance:  $2.3 + j9.5\ \Omega$ .  
 Optimum load impedance:  $4.3 + j8.6\ \Omega$ .  
 Conditions: class-B operation;  $V_{DS} = 24\text{ V}$ ;  
 $I_{DQ} = 20\text{ mA}$ ;  $f = 960\text{ MHz}$ ;  $P_L = 7.5\text{ W}$ ; typical values.

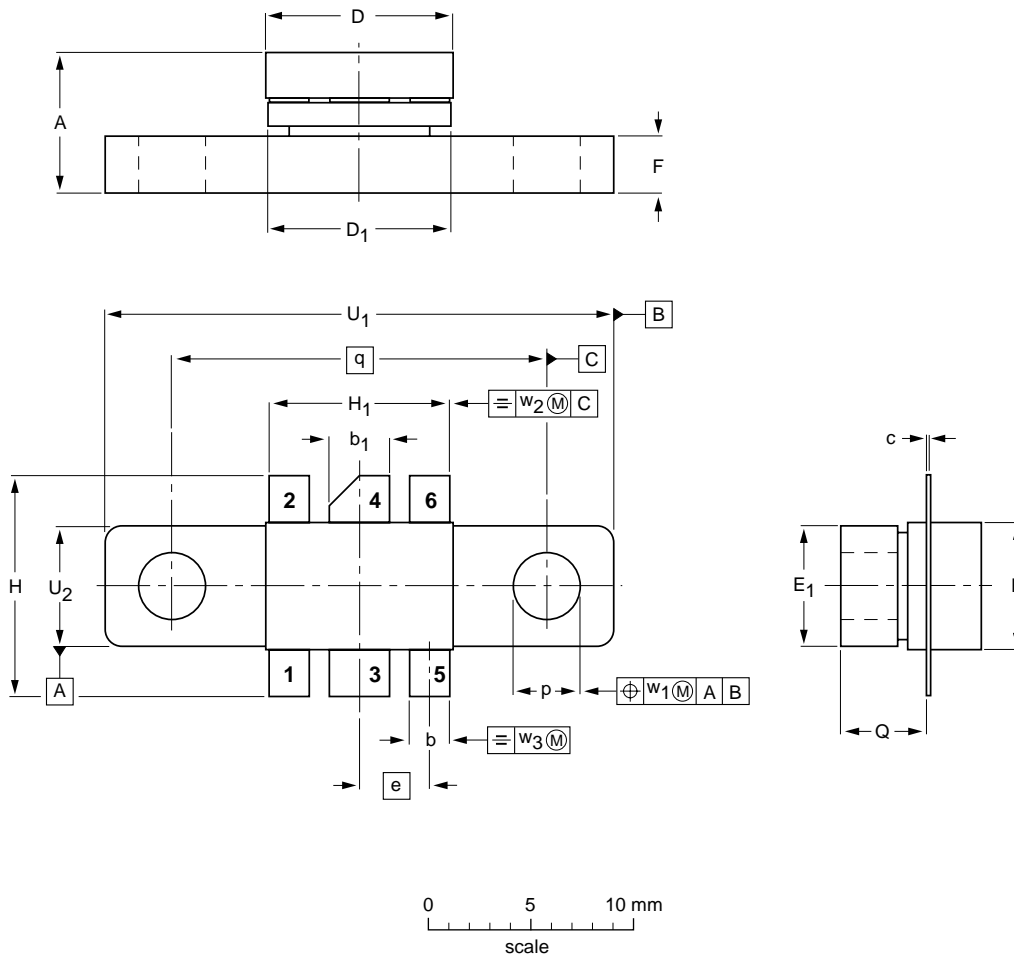
UHF power MOS transistor

BLF543

PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 6 leads

SOT171A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b <sub>1</sub>	c	D	D <sub>1</sub>	E	E <sub>1</sub>	e	F	H	H <sub>1</sub>	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>	w <sub>3</sub>
mm	6.81 6.07	2.15 1.85	3.20 2.89	0.16 0.07	9.25 9.04	9.30 8.99	5.95 5.74	6.00 5.70	3.58	3.05 2.54	11.31 10.54	9.27 9.01	3.43 3.17	4.32 4.11	18.42	24.90 24.63	6.00 5.70	0.51	1.02	0.26
inches	0.268 0.239	0.085 0.073	0.126 0.114	0.006 0.003	0.364 0.356	0.366 0.354	0.234 0.226	0.236 0.224	0.140	0.120 0.100	0.445 0.415	0.365 0.355	0.135 0.125	0.170 0.162	0.725	0.980 0.970	0.236 0.224	0.02	0.04	0.01

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT171A						97-06-28

## UHF power MOS transistor

BLF543

**DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

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